IN THE CLAIMS:

1. (Currently Amended) A high speed processor having:

   (a) a data processing unit for processing data;

   (b) a data memory which is connected to the data processing unit via a data bus and can be addressed by the data processing unit via a data memory address bus in a data address space;

   (c) at least one input interface buffer which is connected to the data bus and has the purpose of buffering input data;

   (d) at least one output interface buffer which is connected to the data bus and has the purpose of buffering output data;

   (e) a ROM memory for storing program data, wherein the ROM memory is connected to the data processing unit via lines; and

   (f) the input interface buffer and the output interface buffer being directly addressable by the data processing unit via [[an]] a separate interface address bus in an independent interface address space.

2. (Previously Presented) The high speed processor as claimed in claim 1, wherein the data memory contains at least one RAM memory.

3. (Canceled)

4. (Currently Amended) The high speed processor ~~as claimed in the claim 1~~ according to claims 1 or 2, wherein the data processing unit is an RISC data processing unit.

5. (Currently Amended) The high speed processor ~~as claimed in claim 1~~ according to claims 1 or 2, wherein the data processing unit contains a plurality of addressable internal registers.

6. (Currently Amended) The high speed processor ~~as claimed in claim 1~~ according to claims 1 or 2, wherein the data processing unit can carry out a plurality of data transfer processor commands in order to directly exchange data between the data memory, the registers and the interface buffers.

7. (Currently Amended) The high speed processor as claimed in claim [[1]] 6, wherein when a first data transfer processor command is carried out by the data processing unit, the input data buffered in the input interface buffer is transmitted directly into an internal register for data processing.

8. (Currently Amended) The high speed processor as claimed in claim [[1]] 5, wherein when a second data transfer processor command is carried out by the data processing unit, the input data buffered in the input interface buffer is transmitted directly into an output interface buffer for the outputting of data.

9. (Currently Amended) The high speed processor as claimed in claim [[1]] 6, wherein when a third data transfer processor command is carried out by the data processing unit, the data buffered in an internal register of the data processing unit is transmitted directly into the output interface buffer for the outputting of data.

10. (Currently Amended) The high speed processor as claimed in claim [[1]] 5, wherein when a fourth data transfer processor command is carried out, the input data buffered in an input interface buffer is transmitted directly into the data memory for storage.

11. (Currently Amended) The high speed processor as claimed in claim [[1]] 9, wherein when a fifth data transfer processor command is carried out by the data processing unit, the data stored in the data memory is transmitted directly into the output interface buffer for the outputting of data.

12. (Previously Presented) The high speed processor as claimed in claim 1, wherein the input interface buffer is connected to an analog/digital converter.

13. (Previously Presented) The high speed processor as claimed in claim 1, wherein the output interface buffer is connected to a D/A converter.

14. (Previously Presented) The high speed processor as claimed in claim 1, wherein the input interface buffer and the output interface buffer are connected to the data processing unit via a control signal bus.

15. (Previously Presented) The high speed processor as claimed in claim 1, wherein the input interface buffer is an xDSL interface buffer for buffer xDSL data.

16. (Previously Presented) The high speed processor as claimed in claim 15, wherein the xDSL input interface buffer has a data frame detecting device for detecting a data frame synchronization data pattern.

17. (Previously Presented) The high speed processor as claimed in claim 16, wherein the data frame detecting device has a shift register for writing in input data, a data pattern memory for storing the data frame synchronization data pattern and a comparator device for bit-by-bit data comparison of the input data written into the shift register, and of the data frame synchronization data pattern stored in the data pattern memory,

the comparator device generating a data frame detection signal if the input data written into the shift register is identical to the stored data frame synchronization data pattern.

18. (Previously Presented) The high speed processor as claimed in claim 17, wherein after the data frame detection signal is generated, the shift register is expanded to form a toroidal memory for buffering the xDSL data.

19. (Previously Presented) The high speed processor as claimed in claim 1, wherein the output interface buffer is a PCM interface buffer for buffering PCM data.

20. (Currently Amended) The high speed processor as claimed in claim [[1]] 5, wherein each internal processor has a plurality of memory locations for different data words.

21. (Currently Amended) The high speed processor as claimed in claim [[1]] 5, wherein each processor task executed by the data processing unit is assigned a separate internal register.

22. (Previously Presented) The high speed processor as claimed in claim 1, wherein peripherals can be connected to the interface buffers.

23. (Previously Presented) The high speed processor as claimed in claim 1, wherein the input interface buffer and the output interface buffer can be configured.